Dynamic Reduction of Power Consumption in Direct-RF Sampling Receivers with Variable Decimation

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Outline

Background and objectives

- Direct-RF sampling and analog RF receivers
- Dynamic reduction of power consumption

Proposed direct-RF sampling receiver

- First-order recursive CIC filter with variable decimation
- Calculated output SNR of ADC followed by CIC filter

Simulations

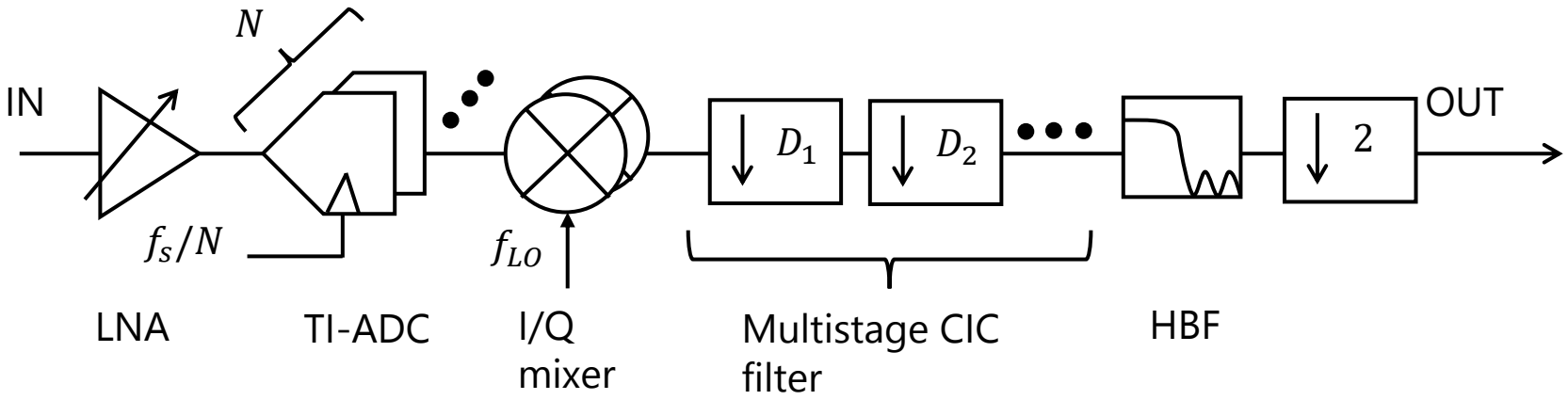
- Output spectrum and SNR (SNR_{out})
- Chip area and power consumption
- Performance comparison

Summary

Background

Direct-RF sampling receivers:

- Consist of LNAs, TI-ADCs, I/Q mixers, CIC filters, and HBFs
- Provide flexibility in designing RF receivers and reduce costs
- Consume much power (~100 mW [1])



Power consumption (P_{DD}) reduced:

- By TI noise-shaping ADC [4], simple I/Q mixer [1], etc.
- According to P_{in} (dynamic reduction), not proposed

LNA: Low-noise amplifier, *N*: Number of channels, TI: Time-interleaved, ADC: Analog-to-digital converter, CIC: Cascaded integrator-comb, *D*: Decimation factor, HBF: Half-band filter, P_{in} : Input power

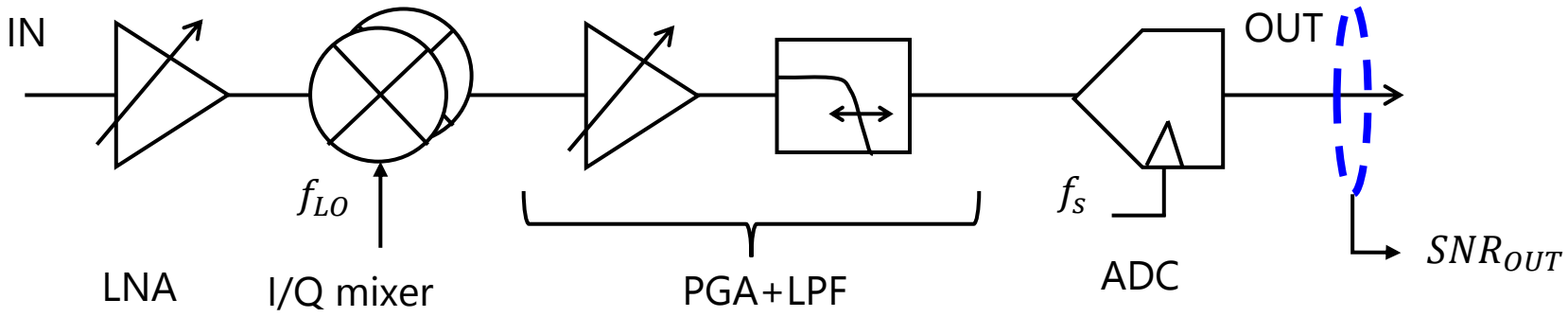
Dynamic Reduction of Power Consumption

WiFi HaLow requirements [6]

$P_{in,min}$ [dBm]		f_{BW} [MHz]	f_{center} [MHz]
BPSK	256-QAM		
-95	-72	1	920

$$SNR_{OUT} = \frac{P_{in}}{P_{RS} \cdot NF}$$

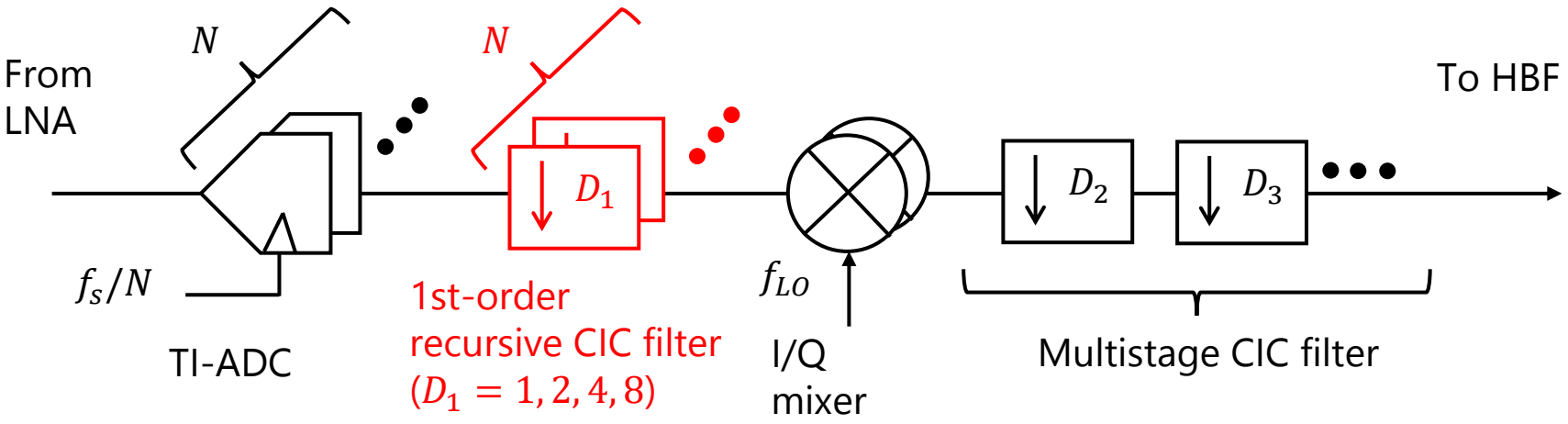
- Receivers can worse NF (reduce P_{DD}) when P_{in} is high.
- Conventional direct-RF sampling receivers can not change NF.
- Analog RF receivers [8, 9] vary the load and feedback resistors in the LNA and LPF, respectively, to adjust the gain.



The conventional RF receivers can not reduce P_{DD} dynamically according to P_{in}.

P_{RS} : Noise power of source resistance, NF: Noise figure

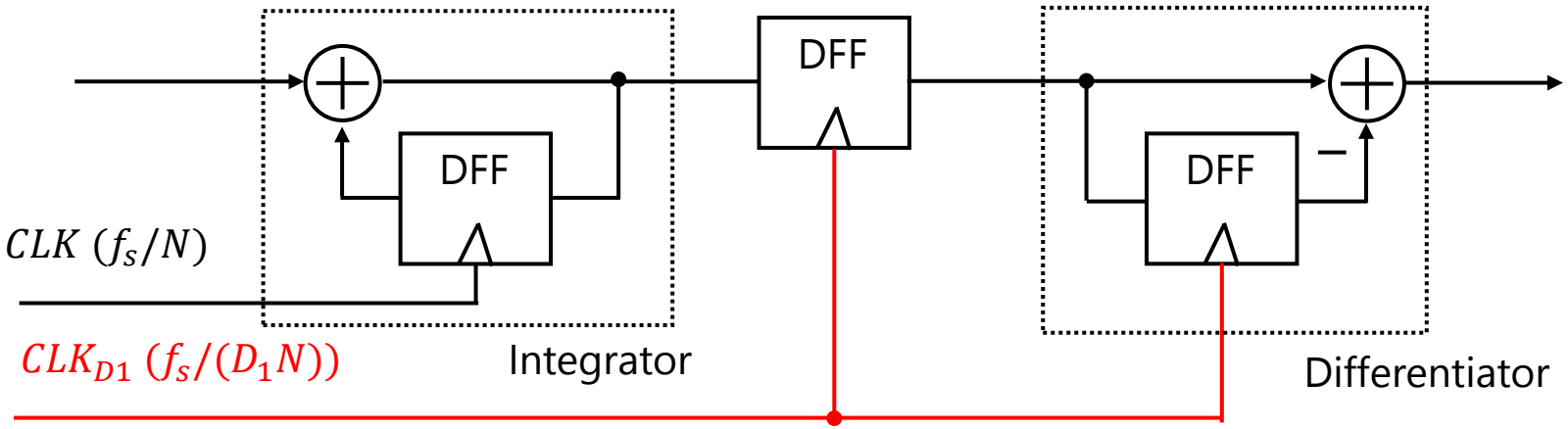
Objectives



Proposed direct-RF receiver decreases:

- Clock frequency of decimators in first-order CIC filters with D_1
- P_{DD} by varying D_1 according to P_{in}
- Folded quantitation noise due to D_1 by using CIC filters

First-Order Recursive CIC Filter with D_1



- The filter consists of an integrator, decimator, and differentiator.
- D_1 is increased by decreasing the clock frequency of DFFs.
- The integrator must operate at f_s/N (a few GS/s), and then L_1 is limited to one.

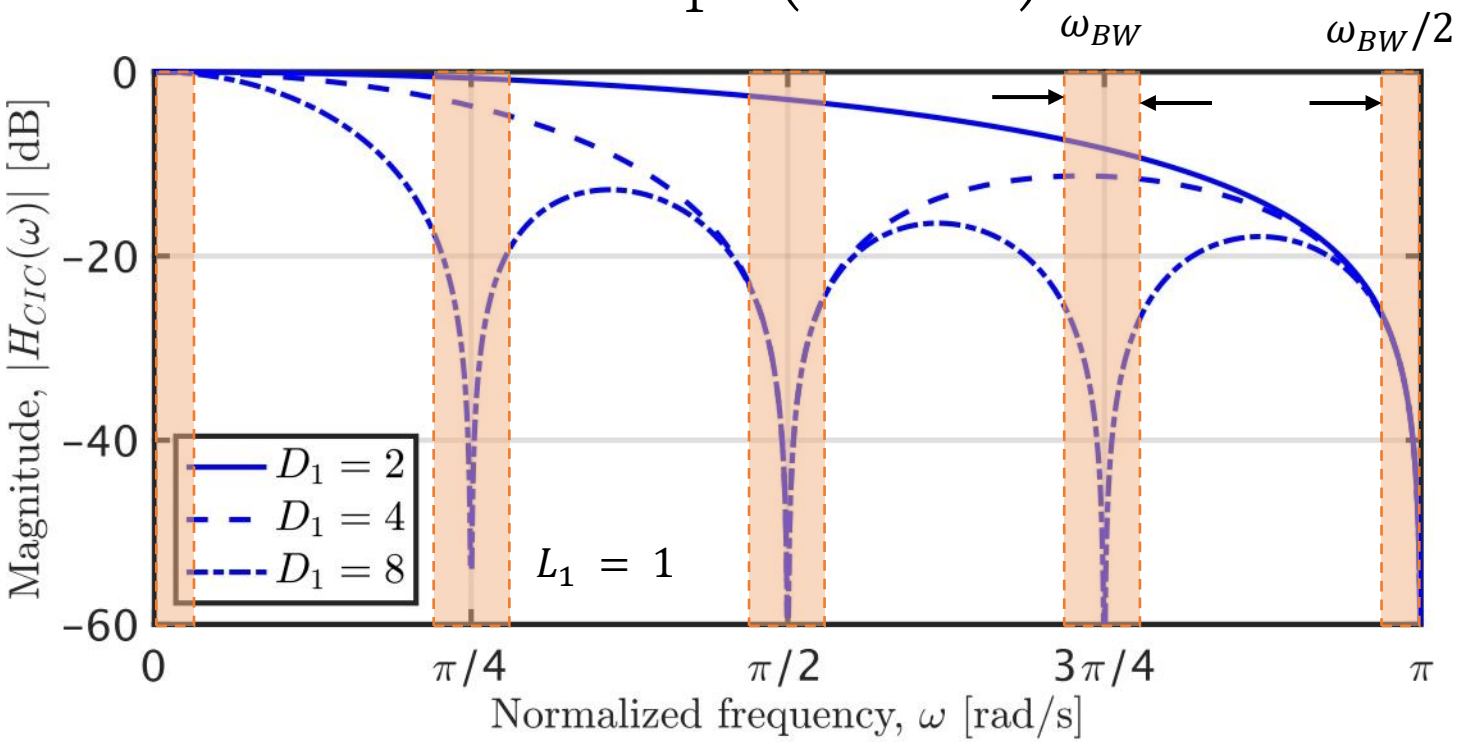
A low L can not reduce the quantization noise of the ADC sufficiently to fold it into ω_{BW} and degrade SNR_{out}.

DFF: D-flip flop, L_1 : Number of stage (order), ω_{BW} : Signal bandwidth, GS/s: Gigasamples per second

Frequency Response of CIC Filter

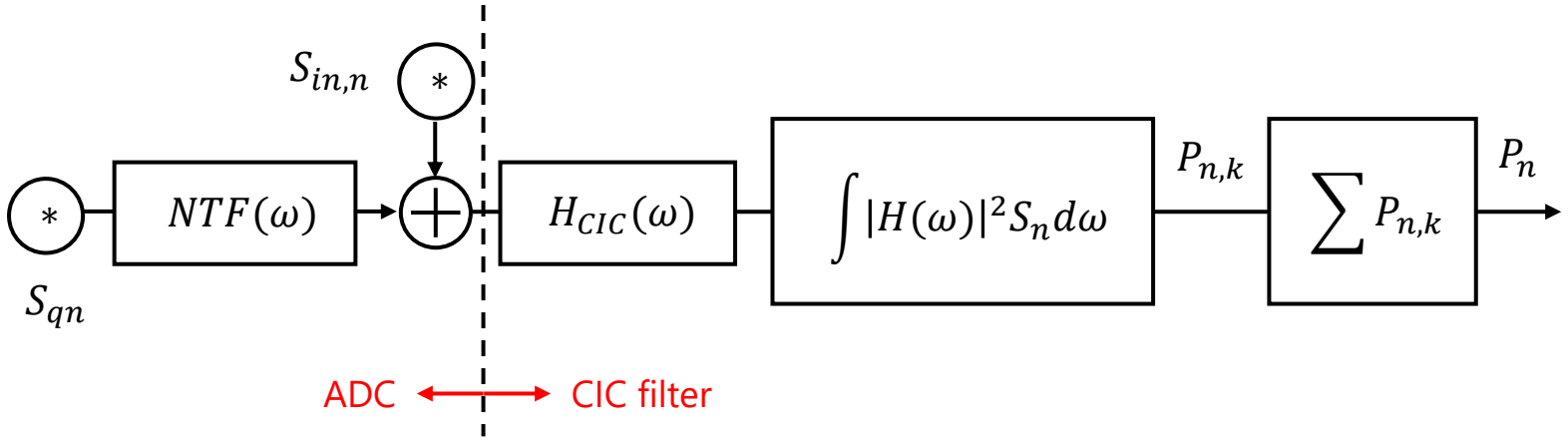
- Transfer function:

$$H_{CIC}(z) = \frac{1}{{D_1}^{L_1}} \left(\frac{1 - z^{-D_1}}{1 - z^{-1}} \right)^{L_1}$$



- The filter folds the noise around $\omega_k = 2k\pi/D_1$ $(k = 1, \cdots, D_1 - 1)$ into ω_{BW} around 0, degrading SNR_{out}.

Noise Model of Noise-Shaping ADC with CIC Filter



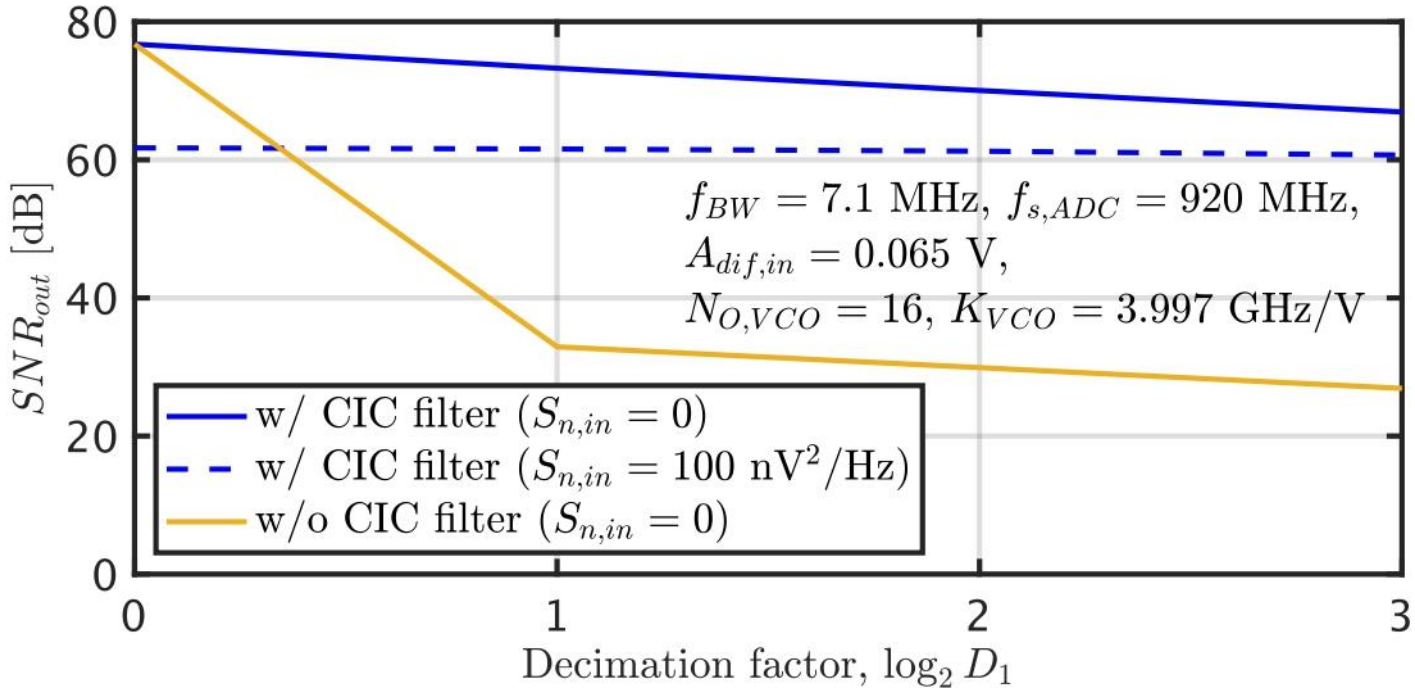
- Quantization noise, S_{qn}, is shaped by $NTF(\omega)$ (Ex. VCO-based ADC).
- Noise from the preceding stages (LNA, T&H, etc.), $S_{in,n}$, is added.
- CIC filter shapes the noise around ω_k, expressed by

$$P_{n,k} = \int_{\omega_k - \frac{\omega_{BW}}{2}}^{\omega_k + \frac{\omega_{BW}}{2}} |H_{CIC}(\omega)|^2 \left(|NTF(\omega)|^2 S_{qn} + S_{in,n} \right) d\omega.$$

- The total noise power, P_n, is given by $\sum_{k=0}^{D_1-1} P_{n,k}$.

VCO : Voltage-controlled oscillator, S_{qn} : Power spectrum density of quantization noise, $NTF(\omega)$: Noise transfer function, T&H : Track and hold

SNR_{OUT} of VCO-based ADC with CIC Filter



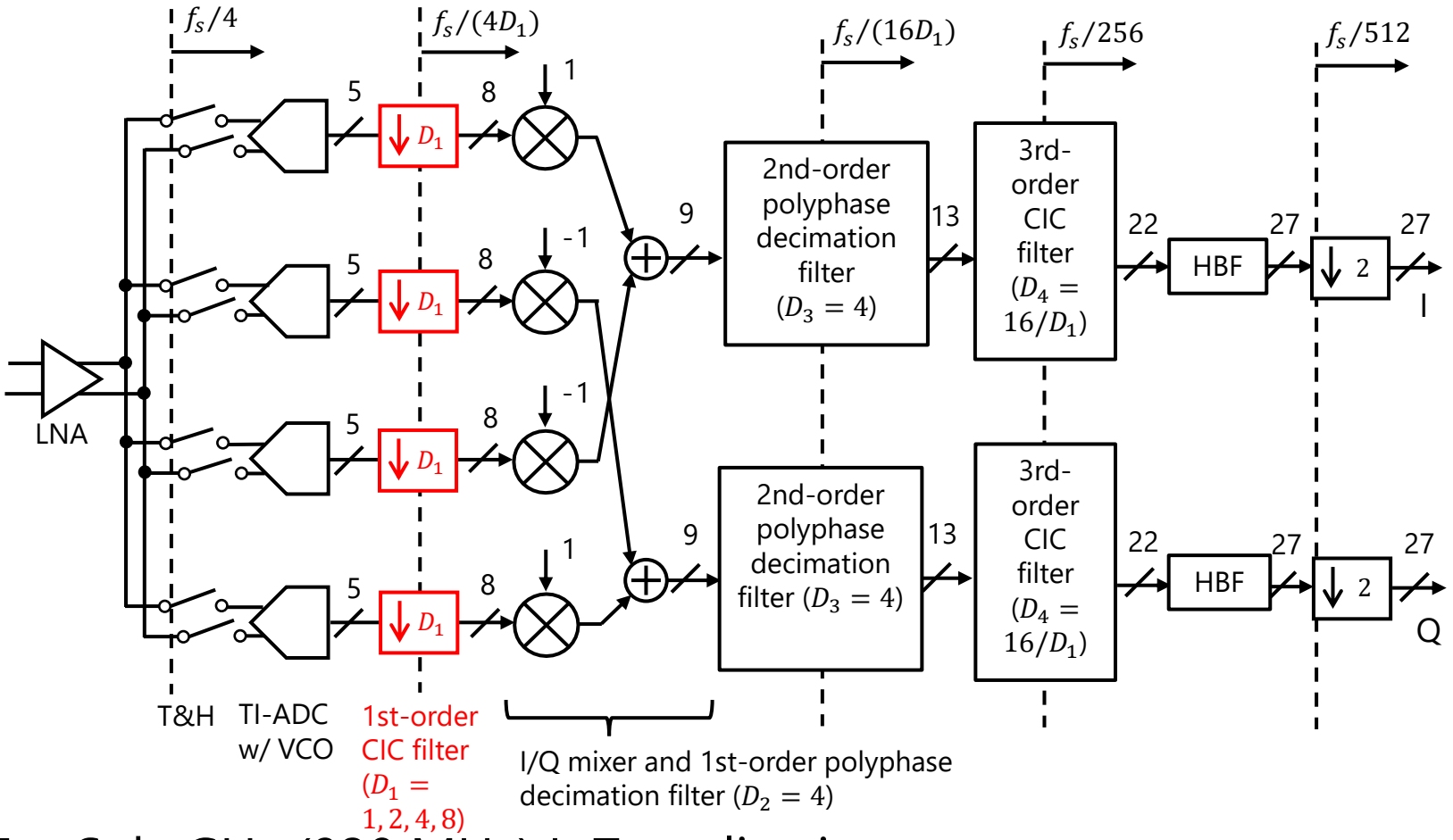
Decimation factor, D_1:

- Degrades SNR_{out} by 3 dB without $S_{n,in}$

The receiver can increase D_1 by two when detecting 3 dB higher P_{in} than $P_{in,min}$.

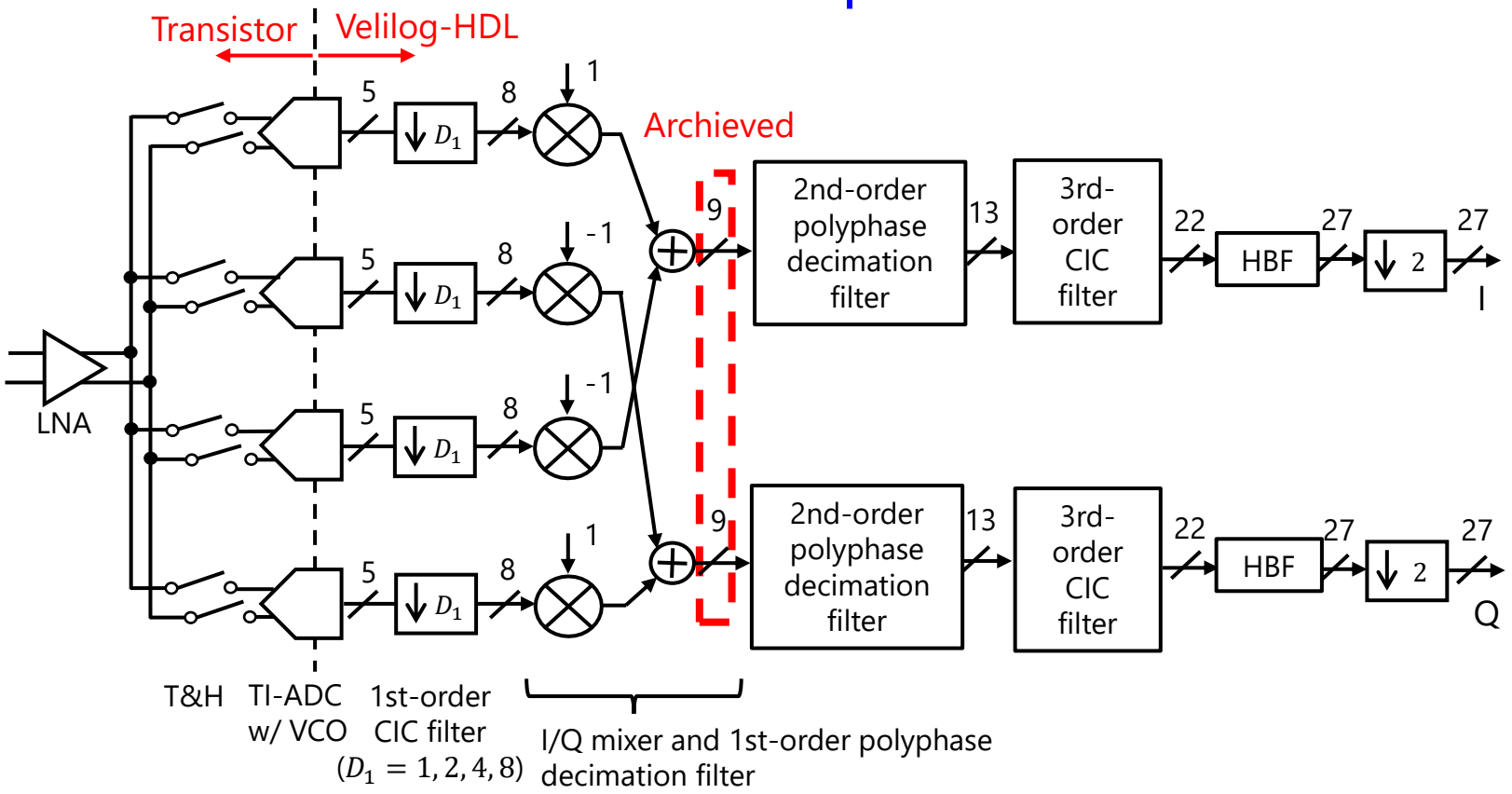
- Does not influence SNR_{out} if $S_{n,in}$ dominates it
- Greatly degrades SNR_{out} without a CIC filter

Block Diagram of Direct-RF Sampling Receiver



- For Sub-GHz (920 MHz) IoT applications
- Consists of LNA, T&H, TI-ADC with VCOs, 1st-order CIC filters ($D_1 = 1,2,4,8$), 2nd-/3rd-order CIC filters, and HBF
- Decreases the data rate of f_s ($= 3680$ MHz) to $f_s/512$ ($= 7.18$ MHz)

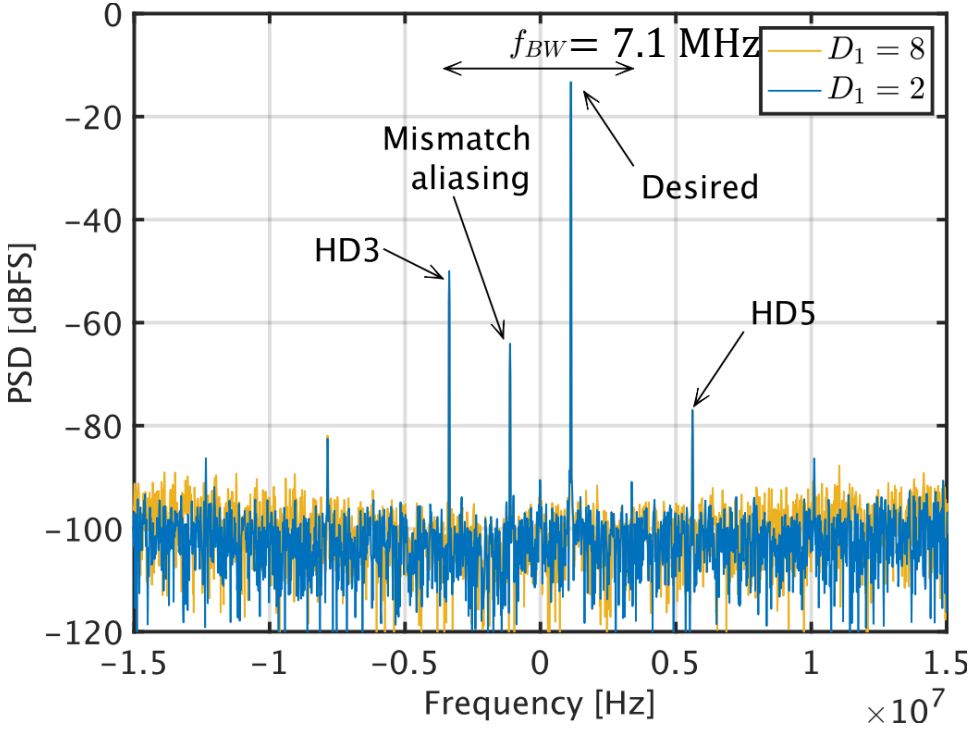
Simulations of Proposed Receiver



- Process, Tools: 65nm CMOS technology, Candence AMS simulator
- Performances: Spectrum (SNR)

Number of data	Input freq. [MHz]	Input Power [dBm]
2^{18}	921.1	-31

Output FFT Spectrum

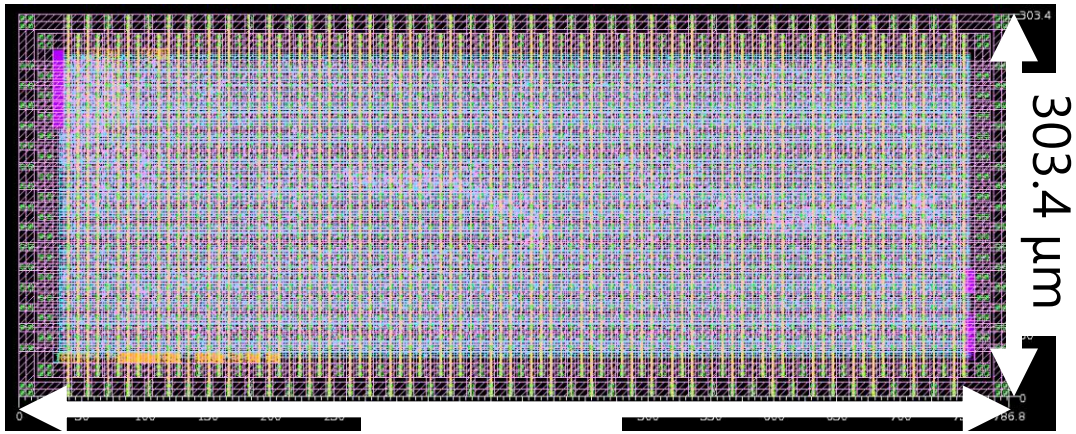


Output	TI-ADC	IQ mixer	
		$D_1 = 2$	$D_1 = 8$
SNR_{OUT} [dB]	62.4	62.3	61.5

- Desired signal was downconverted to 1.1 MHz.
- Mismatch aliasing and HD3/HD5 can be removed by digital correction [11,12].
- D_1 = 2, 8 degraded SNR_{OUT} by 0.1 dB and 0.9 dB, respectively.

HD3: Third-order harmonic distortion , HD5 : Fifth-order harmonic distortion

Layout and Power Consumption of Digital Blocks



- Process: 65 nm CMOS technology
- Tools: Synopsys Design and IC Compiler II
- Condition: (Worst) SS, 0.9-V supply, 125℃ for P&R, (Typ) TT, 1.0 V supply, 25℃ for P_{DD}
- Switching activity set to input and output ports for P_{DD}

f_s [MS/s]	P_{DD} [mW]				Chip area [mm^2]
	$D_1 = 1$	$D_1 = 2$	$D_1 = 4$	$D_1 = 8$	
3680	5.1	4.6	4.3	4.1	0.24

Varying D_1 from one to eight reduces P_{DD} by 1.0 mW.

Performance Comparison of RF Receivers

		This work	E. Martens *et al.* [1]	R. Nanda *et al.* [2]	C. Erdmann *et al.* [3]	A. Ba *et al.* [8]
Architecture		Direct-RF	Direct-RF	Direct-RF	Direct-RF	Zero-IF
Blocks		LNA, T&H, clock gen., ADC, mixer, CIC, HBF	ΔΣADC, clock gen., mixer, CIC, HBF	Mixer, CIC, IP, GC, HBF	ADC, PLL, mixer, NCO, decimators, FIFO	LNA, mixer, LPF, ADC, PLL
CMOS technology [nm]		65	45	65	16 (FinFET)	40
RF center frequency [MHz]		920	2220	1000-2700	3500	755-928
Sampling rate of TI-ADC [MS/s]		3680	8880	2700	4423	N/A
SNDR@BW [dB]		61.5@7.1 MHz	42@80 MHz	72@20 MHz	57.3@2.2 GHz	N/A@1 MHz
Power consumption P_{DD}	Analog/Digital [mW]	5.5 / 5.1 (4.1)	163.5 / 14.3	N/A / 14	424 / 323	4.4 / N/A
	Dynamic reduction	Yes	No	No	No	No
Chip area [mm^2]		0.24	0.4	0.4	>0.45	~1.0
Measured		No	Yes	Yes	Yes	Yes

- The proposed receiver deals with narrower f_{BW} than [1]-[3] to operate with the lowest P_{DD} (10.6 mW for $D_1 = 1$, 9.6 mW for $D_1 = 8$).
- P_{DD} is comparable to that of analog RF receivers [8, 9].

IP: Interpolation, GC: Gain control, NCO: Numerically controlled oscillator

Summary

- We placed first-order recursive CIC filters with variable D_1 after a TI-ADC with VCOs in a direct-RF sampling receiver.
- The CIC filter decreases P_{DD}, whereas increases SNR_{OUT}.
- We designed a 3.6-GS/s direct-RF sampling receiver for Sub-GHz applications by using a 65-nm CMOS process.
- Circuit-level simulations show that the receiver consumes 10.6 mW to achieve an SNR_{OUT} of 61.5 dB.
- The dynamic reduction with variable decimation can reduce P_{DD} by 1.0 mW.