A Standard-cell Based A/D Converter with a Back-gate VCO and a Fat Tree Encoder

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Outline

- Background and objectives

- Proposed VCO-based A/D converter (ADC) with standard cells
  - Back-gate voltage-controlled oscillator (VCO)
  - Sampler
  - Phase detector using fat tree encoder

- Simulation and comparison

- Summary
Background

- **VCO-based ADC**
  - Consists of only digital standard cells ⇒ Low cost and faster time to market
  - Achieves noise shaping ⇒ High signal-to-noise-ratio (SNR)

![Diagram of VCO-based ADC](image)

- **Conventional VCO-based ADC**
  - Changes the oscillation frequency with the supply voltage.
  - Level conversion keeps the output amplitude constant, increasing power consumption.
  - Counter detecting the phase of VCO signal is not suitable for high-speed sampling due to adders (200 MS/s).
Objectives

- **Proposed VCO-based ADC**
  - Back-gate VCO ($N=64$)
  - Keeps its output amplitude constant without level conversion.
  - Phase detector using fat tree encoder
    - Can operate at higher sampling frequencies (800 MS/s), increasing SNR.

We show the effectiveness of the proposed ADC by simulation.
Ring VCO consists of 64 pseudo-differential delay cells.
- Differential input ($V_{b,n} - V_{b,p}$) increases the SNR of the ADC.
- Delay cells consist of NOT gates.
- Oscillation frequency is controlled by the back-gate voltages ($V_{b,p}, V_{b,n}$).
- Generates rail-to-rail (GND–VDD) oscillation signals, because the inverter inherently has a rail-to-rail swing and the back-gate control needs no voltage headroom.
**Output Signals of Back-Gate VCO**

- Back-gate VCO simulated with Cadence Specter RF
  - Input voltage: $0 \sim 750$ mV ($V_{DD}$).
  - Output signals: $0 \sim 750$ mV
  - The output signals can be sampled by digital latches without the level conversion.
  - Oscillation frequency: $184$ MHz $\sim 318$ MHz
    (VCO gain, $K_{vco} = 89.3$ MHz/V)

![Graph showing output voltage vs. time for back-gate VCO](image)
Sampler (Set/Reset Latch)

- Consists of NAND gates.
- Activated by the high level of CLK with a period of $T_s (=1/fs)$, And then, it quantizes the difference between $V_{out,p}$ and $V_{out,n}$ without differential DFFs.

<table>
<thead>
<tr>
<th></th>
<th>CLK</th>
<th>S</th>
<th>R</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>×</td>
<td>×</td>
<td>×</td>
<td>Hold</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

fs: Sampling frequency, DFF: D-flip flop
Phase Detector (4-Stage Ring VCO)

- Finds where the outputs of the ring VCO invert and produces the position in a binary code.

<table>
<thead>
<tr>
<th>From sampler</th>
<th>$Q_{&lt;3:0&gt;}$</th>
<th>$\overline{Q}_{&lt;3:0&gt;}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Thermometer code</th>
<th>$O_{&lt;7:0&gt;}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

Fat tree encoder

$E_{out_{<2:0>}} = \log_2 \overline{O}$

1. NAND gates output a sequence consisting of many 1s and one 0, representing the boundary between 0 and 1 of $Q$.
2. Fat tree encoder outputs the bit position of 0 in a binary code.
Fat Tree Encoder (4-Stage Ring VCO)

- Fat tree encoder can operate at higher sampling frequencies than a ROM-based encoder.
- Delay is an order of $\log_2(B_{in, en})$.
- Operating speed is improved by inserting pippling resistors into each stage.

$B_{in, en}$: Input bit width of encoder

Simulation

- Process: Renesas 65 nm SOTB CMOS
- Supply voltage: 750 mV
- Simulator: Synopsys VCS and XA

Transistor-level

Verilog-HDL (satisfying timing constraints at 800 MHz)

<table>
<thead>
<tr>
<th>Input amplitude $A_{in}$ [mV]</th>
<th>Input frequency $f_{in}$ [MHz]</th>
<th>Input common voltage [mV]</th>
<th>Clock frequency $f_s$ [MHz]</th>
<th>OSR</th>
<th>Sampling points</th>
</tr>
</thead>
<tbody>
<tr>
<td>750</td>
<td>4.882</td>
<td>375</td>
<td>800</td>
<td>20</td>
<td>16384</td>
</tr>
</tbody>
</table>

SOTB : Silicon on thin buried oxide
The SNR of the ADC was evaluated by the simulated output spectrum achieved by FFT on MATLAB. 

- SNR (simulated) = 57.9 dB, SNR (theoretical) = 56.2 dB
- Nonlinearity of $K_{vco}$ causes harmonics (SNDR = 19.7 dB)

$$\text{SNR} \approx 6.02 \log_2(2A_{in}K_{VCO}N_{st}/f_s) + 2.61 + 30 \log \text{OSR} \, [\text{dB}]$$

$K_{vco} = 89.3 \text{ MHz/V}$, number of VCO stage, $N_{st} = 64$
## Comparision

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<thead>
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</tr>
</thead>
<tbody>
<tr>
<td>TCAS-I’14 [2]</td>
<td>200</td>
<td>25.62</td>
<td>52.8</td>
<td>50.3</td>
<td>8.06</td>
<td>3.3</td>
<td>151.7</td>
</tr>
<tr>
<td>JSSC’17 [3]</td>
<td>1600</td>
<td>10.0</td>
<td>66.2</td>
<td>65.7</td>
<td>10.6</td>
<td>3.7</td>
<td>111</td>
</tr>
<tr>
<td>This work</td>
<td>800</td>
<td>20.0</td>
<td>57.9</td>
<td>18.7</td>
<td>2.81</td>
<td>2.7</td>
<td>105</td>
</tr>
</tbody>
</table>

\[
FoM = \frac{P_{DD}}{2^{(SNR-1.76)/6.02}} \cdot 2\cdot BW
\]

\[
ENOB = \frac{SNDR-1.76}{6.02}
\]

- Proposed ADC obtained the best FoM among the ADCs.
- SNDR was the lowest due to harmonics.

FoM: Figure of merit \hspace{1cm} ENOB: Effective number of bits \hspace{1cm} $P_{DD}$: Power consumption
Summary

- 800-MS/s ADC with a back-gate VCO and a fat tree encoder
  - All blocks consist of digital standard cells.

- Back-gate VCO generates rail-to-rail output signals, requiring no level conversion.

- Phase detector using a fat tree encoder can operate at higher sampling frequencies than detectors based on counters.

- Simulated SNR (57.9 dB) corresponds to the theoretical value (56.2 dB).

- Obtained Best FoM among previously reported ADCs.